In the Claims

Please cancel claim 1.

Please add the following claims 2-25:

2. (New) A modulator, comprising:

a delay circuit receiving a native pixel clock and outputting multiple subclocks at multiple different positions within the same native pixel clock period; and

a skew pulse generator outputting multiple subpixels during each native pixel clock period according to the multiple output subclocks.

3. (New) A modulator according to claim 2 wherein the digital delay circuit outputs N subclocks for each clock period of the native pixel clock, where N is an integer.

4. (New) A modulator according to claim 2 wherein the skew pulse generator includes a pulse generator for generating multiple differently skewed clock pulses from the subclocks within each native pixel clock period, the different clock pulses each controlling the output for an associated one of the subpixels.

5. (New) A modulator according to claim 4 wherein the pulse generator comprises multiple AND gates that logically combine different subclock combinations together to form one of the clock pulses.

6. (New) A modulator according to claim 4 wherein the skew pulse generator includes output buffers each receiving an associated one of the subpixels and output enabled by an associated one of the clock pulses.

7. (New) A modulator according to claim 6 wherein the buffers comprise tri-state buffers.

8. (New) A modulator according to claim 2 including a first set of registers supplying a first half of the subpixels to the skew pulse generator after a falling edge of the native pixel clock signal and a second set of registers supplying a second half of the subpixels to the skew pulse generator after a rising edge of the native pixel clock signal.

9. (New) A modulator according to claim 2 including:

an associative shift register generating addresses associated with pixel values; and

a look-up table coupled between the associative shift register and the skew pulse generator, the look-up table generating subpixels for the pixel values according to the associated address.

10. (New) A modulator according to claim 9 wherein the associative shift register is programmable to generate the addresses according to a selectable number of bits associated with each pixel value.

11. (New) A modulator according to claim 10 wherein the associative shift register varies a number of pixel values combined to generate the addresses according to the number of bits associated with each pixel value.

12. (New) A modulator according to claim 2 including:

a literal mode shift register outputting a number of bits each representing a pixel value of an image to be printed which in turn becomes a subpixel relative to the native clock period; and

a bit expander expanding each one of the bits output from the shift register into a group of subpixels relative to the native clock period.

13. (New) A modulator according to claim 12 wherein the literal mode shift register and the bit expander are programmable to generate a selectable number of subpixels for each pixel value thereby varying dot per inch pixel resolution.

14. (New) A modulator according to claim 2 including a clock skew synchronizer coupled to the skew pulse generator for aligning the subpixels with a line synchronization signal.

15. (New) A modulator according to claim 14 wherein the clock skew synchronizer includes the following:

multiple registers having data inputs coupled to the different subclocks output from the digital delay circuit, clock inputs coupled to the line synchronization signal and data outputs;

an edge detector coupled to the data outputs of the multiple registers, the edge detector generating a shift value according to which of the subclocks is first clocked into the multiple registers by the line synchronization signal; and

a shift register shifting the subpixels into the skew pulse generator according to the shift value.

16. (New) A method for aligning subpixels with a line synchronization signal comprising:

generating multiple subclocks at different percentages of a native pixel clock period;

identifying a first one of the subclocks active when the line synchronization signal is initially asserted;

generating a shift value according to the identified one of the subclocks; and

shifting the subpixels according to the shift value.

17. (New) A method according to claim 16 including shifting out the subpixels according to the shift value during the native clock period and outputting any remaining subpixels during a next clock period of the native pixel clock.

18. (New) A method according to claim 16 including:

generating the multiple subclocks at multiple different positions within the native pixel clock period;

generating different clock pulses by combining different combinations of the subclocks together; and

generating multiple subpixels within the native pixel clock period by generating the subpixels according to the multiple clock pulses.

19. (New) A method for generating subpixels in a print engine, comprising:

generating multiple subclocks each skewed to multiple different positions within the native pixel clock period;

generating different clock pulses for each native pixel clock period by combining different combinations of the subclocks together; and

generating multiple subpixels within the native pixel clock period by generating the subpixels according to the multiple clock pulses.

20. (New) A method according to claim 19 including:

generating address values according to a selectable bit per pixel mode that varies a number of bits associated with a center native pixel and varies a number of native pixels preceding and following the center native pixel; and

outputting subpixels associated with the center native pixel according to the address values.

21. (New) A method according to claim 20 including:

receiving bits each associated with one of the native pixels;

outputting the bits in selectable sized groups for each native pixel clock period; and

expanding each bit in the group into one or more subpixels, the number of subpixels expanded from each bit varying according to the number of bits in the group.

22. (New) A method according to claim 19 including:

latching the subclocks according to a line synchronization signal;

generating a shift value according to which subclocks were latched by the line synchronization signal; and

shifting the multiple subpixels into alignment with the line synchronization signal according to the shift value.

23. (New) A clock skew synchronizer for aligning subpixels in a print engine with a line synchronization signal comprising:

a digital delay circuit outputting multiple subclocks according to a native pixel clock signal, the multiple subclocks each skewed at multiple different percentages of the native pixel clock period;

multiple registers each having a data input coupled to a different one of the subclocks for shifting subpixel values to multiple different subpixel percentages within the same native pixel clock period;

an edge detector coupled to data outputs of the multiple registers, the edge detector generating a shift value according to which of the multiple registers first detect actuation of the line synchronization signal; and

a shift register shifting the subpixels into alignment with the line synchronization signal according to the shift value.

24. (New) A clock skew synchronizer according to claim 23 including a remainder circuit outputting the subpixels not shifted out of the shift register during a next clock period of the native pixel clock.

25. (New) A clock skew synchronizer according to claim 23 including a skew pulse generator receiving the multiple subclocks from the digital delay circuit and the shifted subpixels from the shift register and outputting the shifted subpixels according to the multiple subclocks.